Abstract—Smart systems consist of heterogeneous subsystems and components providing different functionalities; they are normally implemented as Multi-Package on a Board. To fully exploit the potential of current nanoelectronics technologies, as well as to enable the integration of existing/new IPs and More than Moore devices, smart system miniaturization and Multi-Chip in a Package implementation are unavoidable. Such goals are only achievable if dedicated EDA flows and tools for smart subsystems/components design and integration are available to designers and system integrators. This paper offers an overview of the major challenges, as perceived from the industrial point of view, to be faced when pursuing effective smart system design capabilities, discussing and motivating the needs and the market opportunities attached to the set-up of automated system design frameworks.

I. THE CONTEXT

Smart systems represent a broad class of systems that can be defined as intelligent, miniaturized devices incorporating functionalities like sensing, actuation, and control; they are usually energy-autonomous and ubiquitously connected. In order to support these functions, they must include sophisticated and heterogeneous components and subsystems such as: Application-specific sensors and actuators, multiple power sources and storage devices, intelligence in the form of power management, baseband computation, digital signal processing, power actuators, and subsystems for various types of wireless connectivity (see Figure 1).

![Smart System Architectural Template](image)

Fig. 1. Smart System Architectural Template.

Smart components and subsystems are clearly developed and produced with very different technologies and materials. Then, the challenge in the realization of such smart systems goes beyond the design of the individual components and subsystems (an already difficult task by itself), but rather in accommodating a multitude of functionalities, technologies, and materials; as such, they involve solving problems of different nature. The widely acknowledged keyword in smart system design is therefore integration.

There are, in practice, two dimensions of integration that represent the main obstacle towards mainstream design of smart systems: Technological and methodological. As already experienced in other domains (e.g., digital and analog design), a solution has been found first for the technological issues. Advanced packaging technologies such as System-in-Package (SiP) and chip stacking (3D IC) with through-silicon vias allow today manufacturers to package all this functionality more densely, combining the various domains depicted in the figure above in a single package. SiP technology works nicely because it allows merging components and subsystems with different processes, and mixed technologies using the state-of-the-arts advanced IC packaging technologies with minor impact on the IC chip design flow.

Unfortunately, design methodologies are falling behind: Current smart system design approaches use separate design tools and ad hoc methods for transferring the non-digital domain to that of IC design and verification tools, which are more consolidated and fully automated. This solution is clearly suboptimal and cannot respond to challenges such as time-to-market and request of advanced sensing functionalities. A big step towards effective large-scale design of smart systems would be that of changing the design of such systems from an expert methodology to a mainstream (automated, integrated, reliable, and repeatable) design methodology, so that design costs are reduced, time-to-market is shortened, design of the various domains is no longer confined to teams of specialists inside IDMs and system miniaturization can be achieved with limited risks.

This objective can be met by defining and implementing a structured design approach that explicitly accounts for integration as a specific constraint, thus minimizing manual hand-off. The ability of exchanging a wide range of complex design parameters between components and subsystems from different technologies, packages, and architectural templates in a holistic co-design framework is an extraordinary challenge, which requires closing several technical and cultural gaps by means a multidisciplinary approach. The task of constructing a flexible modeling, simulation, design and integration software platform for miniaturized smart systems is thus very ambitious and requires the investment of specific know-how, the availability of human and financial resources and the effort of a large team of dedicated and motivated researchers, scientists and engineers with multidisciplinary and complementary competences.
II. STATE OF THE ART IN SMART SYSTEM DESIGN

For the modeling, simulation, design and integration of smart systems, the scenario we face today is the following:

- The non-electrical parts (micromechanical structures, electromagnetic fields, thermal phenomena, wave propagation etc.) are designed using Partial Differential Equations (PDE) solvers, like the Finite Element Method (FEM), or, alternatively, schematic-based behavioral libraries.
- The analog and RF parts are designed based on reuse of existing macros by experienced engineers, following a template-based approach.
- The digital parts are designed using highly automated synthesis tools (from high-level synthesis to physical synthesis) following a top-down paradigm.
- System design is supported by block diagram simulation (e.g., MATLAB-SIMULINK) or newer approaches, which allow to obtain a comprehensive view of the entire system, yet through simple models of the subsystems and of the components.
- The amount of software, implemented in microcontrollers and DSPs, is significantly increasing, in-line with the trend that can be observed in embedded-system design.

A. Abstraction Levels

In order to provide a clear framework for categorizing methodologies and tools, which are adopted in smart system design, it is worth distinguishing between the different levels of design abstraction: System level, device level and physical level.

a) System Level.: The interactions of the heterogeneous components and subsystems, for example MEMS or power sources, with their environment and control electronics can be modeled and simulated at the system level of abstraction. Models at this level can include not only power sources, RF, MEMS and analog parts, but also digital macro-cells and software.

b) Device Level.: Circuit simulation programs, such as SPICE and derivatives, are used for device or circuit level design. A netlist describes the circuit elements (e.g., transistors, resistors, capacitors) and their connections, and translates such description into non-linear differential equations to be solved using implicit integration methods, Newton’s method and sparse matrix techniques.

c) Physical Level.: Power sources, sensors, MEMS and other discrete devices have traditionally been modeled using 3D field solvers based on the finite element method (FEM) and boundary element method (BEM). These approaches, which can be described as physical modeling, entail decomposing the device geometry into a collection of volume or surface elements (meshing), and then solving a system of partial differential equations for the field values at the element control points. Today, a variety of single-physics and multi-physics field solvers is available, ranging from general-purpose tools to those that address MEMS-specific physics such as electrostatic sensing and actuation, piezo-electric effects, and gas damping.

B. Limitations of Current Design Approaches

Today, different kinds of design tools exist: Board/module level, electronic circuit design level and physical level. The design of a smart system (implemented as a SiP) that deals with embedded systems generated from bare die requires a strong link between these different worlds. The tight integration of such differing systems sets high requirements on the system design flow. While FEM (Finite-Element-Method) simulation allows analyzing detailed problems, models for higher abstraction levels are needed to exceed the complexity barrier imposed by the need of dealing with electrical, electromechanical and thermal interfaces.

The design and simulation frameworks for component/subsystem integration created by system integrators are non-standard and show several of limitations:

- Very fragmented (stitching of bits and pieces of existing EDA tools and flows from different vendors). Very fragile (scripting, tool interfacing, data formatting).
- Expensive (licensing from different vendors).
- Not flexible (changes in system architecture, building blocks, models and workloads often imply significant revision of the framework).
- Customized to specific applications (application domains).

III. CHALLENGES IN AUTOMATED SMART SYSTEM DESIGN

The main issues and research objectives for a multi-level design methodology for smart systems include:

- Coupling of physical effects, chemistry, and biology towards multi-domain modeling approaches.
- Consideration of non-linear effects and structural discontinuities supported by efficient modeling and simulation algorithms.
- Simultaneous handling of different physical paradigms in one physical domain. For instance:
  - Fluidics: Continuum mechanics and molecular interactions
  - Electromagnetic fields: Low frequencies and RF/wave propagation depending on structural dimensions and signal frequencies.
- Consideration of technological issues in early design phases and at system-level:
  - Packaging: thermal effects and their influence on function and reliability
  - Process capabilities: inadequate shaping of microstructures in manufacturing causes modified system behaviour (e.g., additional mechanical stress) or parasitic effects.
  - Process characterization: Design centering/yield enhancement.
- Co-design and co-simulation of electronics (e.g., analog, digital) with non-electronics (e.g., MEMS, power sources) over multiple scales.
- IP transfer and provision for heterogeneous microsystem components.
The domains and abstraction levels that must be considered in a comprehensive modeling framework for smart system design and integration can be pictorially summarized as in Figure 2.

Fig. 2. Domains and Abstraction Levels in Smart System Design.

We can divide the design engineers into different groups: The MEMS engineers, the IC engineers and the system architects. All groups frequently express the need to co-simulate their component designs in a common simulation environment. Co-simulation is required to verify the IC design and to predict yield sensitivity to manufacturing variations. One obvious path is to do the co-simulation in the environment used by the IC designers. This requires that the MEMS designers deliver a behavioral model of the MEMS devices expressed in a suitable hardware description language (HDL) such as Verilog-A or VHDL-AMS. Today, MEMS engineers have very limited ability to deliver behavioral models in these formats. Very often they build the model manually, usually in the form of a look-up table, or generate a Reduced-Order Model (ROM) from finite element analysis.

The drawback of the existing ROM techniques is that those algorithms can only analyze a single model configuration with specified dimensions and physical parameters. In practice, there is necessity to know the influence of parameter variations on the modal response of the structure in order to optimize the entire system and to assess the effect of tolerances or changed material. Beyond the commercial software, there is often the use of advanced computational approaches for extending the considered effects within the ROM methods. Different types of design parameters can be handled in modeling of MEMS components. The most obvious ones are continuous parameters such as geometrical dimensions, material properties, etc. Process issues involving dimensional variations can highly change the transfer function of the MEMS components as well as have an influence on the effect of temperature and packaging.

The lack of IC-compatible parametric MEMS behavioral models is an impediment to design reuse and to the licensing of MEMS IP. The availability of a library of validated MEMS design IP in the environment that a IC designer or system architect is used to work in, would revolutionize the way smart based system are developed today.

There is very limited ability to deliver MEMS component models for architectural level design. System engineers are usually required to hand craft non-parametric models or look-up tables from publicly available data sheets. System-level tools such as Simulink are often used for functional modeling and simulation. They may also capture continuous-time behaviour, but do not target the design of Embedded-AMS (E-AMS) systems at an architecture-level. Hardware description languages (HDLs) target the design of mixed-signal subsystems close to implementation level, but these languages have limited capabilities to provide efficient HW/SW co-design at high level of abstraction. Existing co-simulation solutions mixing SystemC and Verilog/VHDL-AMS do not provide high enough simulation performance and lack offering a seamless design refinement flow for modeling mixed discrete-event/continuous-time systems and HW/SW systems at architectural level. In conclusion component models are not yet integration aware.

IV. IMPACT OF AUTOMATED DESIGN

A. Smart Systems Market: Facts and Perspectives

The growth of miniaturized smart systems market is an attractive opportunity to positively impact the European economy and industry. In 2008, the global market was evaluated at about USD 50B and it is expected to grow to USD 200B in 2020 (source: Yole Development). Smartphones success story is just a beginning; more will come. If largest growth is expected in consumer and diagnostic applications, miniaturized smart systems find applications in a broader range of key strategic sectors, including: Automotive, healthcare, Internet of Things, safety and security and aerospace. Also, efficient energy management and environment protection are business sectors in which the utilization of miniaturized smart systems may make a difference. The worldwide market for monitoring & control products and solutions, one of the most important fields of smart systems applications, containing solutions for environment, critical infrastructures, manufacturing and process industry, buildings and homes, household appliances, vehicles, logistics & transport or power grids, is around Euro 188B. This value represents 8% of the total ICT expenditures world-wide, and it is identical to the whole semiconductor industry world revenues and approximately twice that of the world mobile phone manufacturers revenues.

The data from the brief market analysis shown above are convincing enough to conclude that the ability of quickly designing high-quality smart systems will offer a strategic advantage over the competitors to the owners of design capabilities.

B. EDA Market: Facts and Perspectives

Over the previous decade, the EDA market has seen a consistent year-on-year growth; and despite the recession, the investments continued till early 2008. Further, a slowdown in investments in the last quarter of 2008 and in 2009 was observed due to the prevailing global economic conditions. As a result, many customers have reduced, deferred or cancelled their investments in the EDA applications. In addition, they
have also reduced or terminated the on-going paid maintenance for their installed base, which negatively impacted the companies recurring revenue. However, there has been a recovery in the EDA applications' market during 2010, as the companies are slowly recovering from the recession and invest in solutions that will provide them a sustainable business advantage and profitability.

Many of the EDA companies are acquiring small companies with software or other technology that can be adapted to their core business. Most of these companies are rather amalgamations of many smaller companies. Further, this trend is helped by the tendency of software companies to design tools as accessories that fit naturally into a larger vendor’s suite of programs (many new tools incorporate analog design, and mixed systems on digital circuitry). This is basically driven by the trend to place the entire electronic systems on a single chip.

The past years and forecast picture has shown a regenerated EDA market in the 2010. There was a -16.6% decline in 2008 and the EDA market raised by only by 1% in 2009. Thanks to the 2010 semiconductor industry growth, EDA growth has accelerated in 2010 (10%) and will certainly keep a healthy range in the coming years. Spending on design tools will once more become a priority; the need for advanced design technology is just too great in this era of rapidly shrinking design features, burgeoning complexity of the design, and manifestation of unexpected physical effects, such as process variations, thermal gradients and reduced manufacturability. Apart from the general macroeconomic conditions, what it is driving the future prospects for the EDA market is development of cutting-edge design technologies that will enable the electronics industry to take advantage of the most advanced design methodologies, processes, and materials. Though new tools have been introduced in the past few years, many methodology transformations remain yet to be introduced. This is mainly due to the evolution of the nanoelectronics technology, which is going to be boosted by the massive R&D effort which will take place in the short term. Therefore, it is incumbent on the EDA industry to maintain its focus on fully developing the next generation of design tools, which should be capable of addressing the challenges that the nanoscale electronic devices will present.

Referring to the specific case of methods and tools for smart system integration, at the moment many of the major EDA companies are focusing primarily on design flows and tools for logic devices, which make up 75% of the world market. Specific tools exist for board design and package design, but they are not integrated with chip design, and nothing is available for System-in-Package integrated design. Support for non-purely logical functions is also poor and limited to RF design and analog/mixed mode design, with severe limitations for complex devices. Big companies normally use in-house developed partial solutions, which present standardization and support problems. The picture above, paired with an overall healthy status of the EDA vendors, highlights great opportunities for business growth by the EDA players that will be quick enough to enter the game of new design methods and tools for smart system integration.

V. CONCLUSIONS

Developing effective smart system design capabilities, methodologies, flows and tools is crucial to enable massive deployment of smart systems in a wealth of business sectors. Several efforts are being undertaken jointly by academia and industry in the R&D landscape to address these objectives, and thus allow designers of smart systems to master, simultaneously and in a seamless manner the challenges that arise when new products need to be conceived and implemented. Among the many initiatives in this domain, it is worth mentioning EPoSS, the European Technology Platform on smart system integration [1]; EPoSS is an industry-driven policy framework that defines R&D and innovation needs, as well as policy requirements related to smart systems integration and integrated micro- and nanosystems. The initiative is of immediate importance in view of defining research and technology priorities in the domain of Smart Systems integration for the EUs FP7, for raising more critical mass and resources and for coordinating between different funding initiatives. The EPoSS Strategic Research Agenda states that future research priorities for Smart Systems integration can be clustered into: Technologies, functionalities and methodologies. Technologies and functionalities need to be combined to build innovative smart systems. Methodologies are the process-oriented dimension encompassing applications as well as technologies and functionalities. More specifically, selected R&D topics of high relevance for smart system integration in the methodologies domain include: Design tools and approaches, simulation of multi-domain systems and components at all levels of abstraction, standards, robustness, quality and reliability.

At the moment, EPoSS is not in the position of defining its own policies for funding relevant R&D initiatives and projects. Therefore, financial support to R&D activities implementing the priorities of the EPoSS Strategic Research Agenda can happen, mainly, through FP7. In this context, we would like to mention an on-going R&D project (the SMAC project [2]), funded within FP7, whose main goal is the implementation of a flexible software platform for smart subsystems/components design and integration is made available to designers and system integrators. The platform will include methodologies and EDA tools enabling multi-disciplinary and multi-scale modeling and design, simulation of multi-domain systems, subsystems and components at all levels of abstraction, system integration and exploration for optimization of specific metrics, such as power, performance, reliability and robustness. We believe that the SMAC project will contribute in a decisive way to the development of smart system design and integration capabilities, thus offering to semiconductor vendors, system integrators and design houses a competitive advantage in aggressively targeting existing and new markets for which innovative smart systems will constitute an enabling technology for new generations of electronic applications.

REFERENCES